

2/20AMBA[31:01]MBUS[31:01]SBUS[31:01]

(A)

(B)

(C)

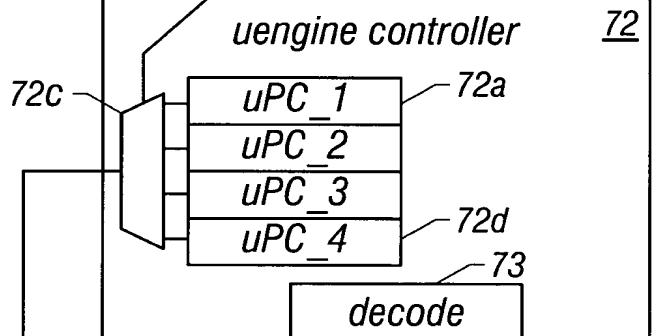
22a →

(D)

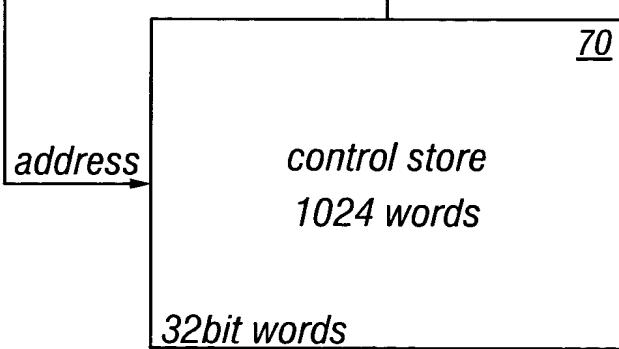
SEQ#_event_response
FBI_event_response
sram_event_response
sdram_event_response
amba_event_response

Context Event Arbiter

74



E



F

FIG. 2A

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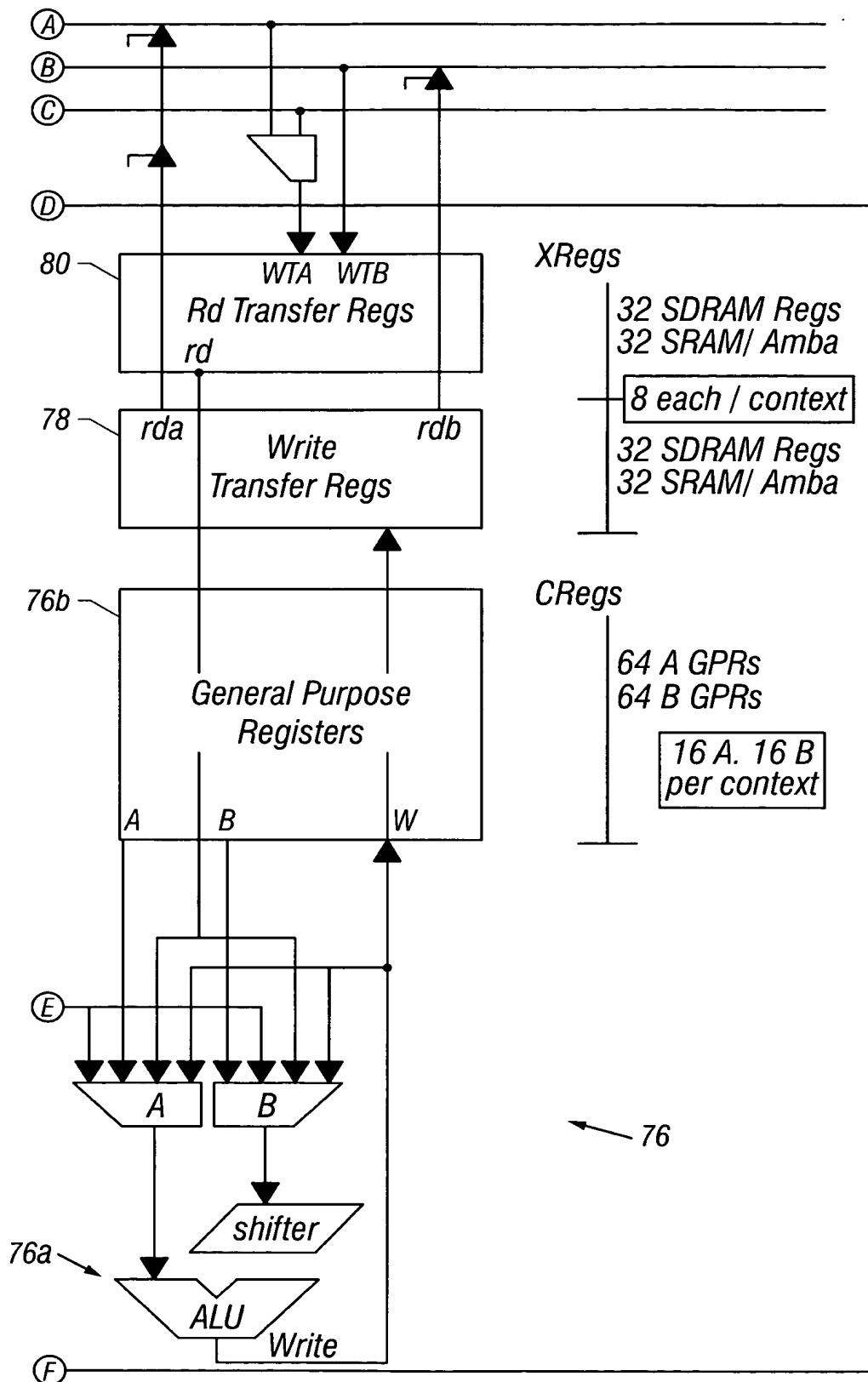


FIG. 2B

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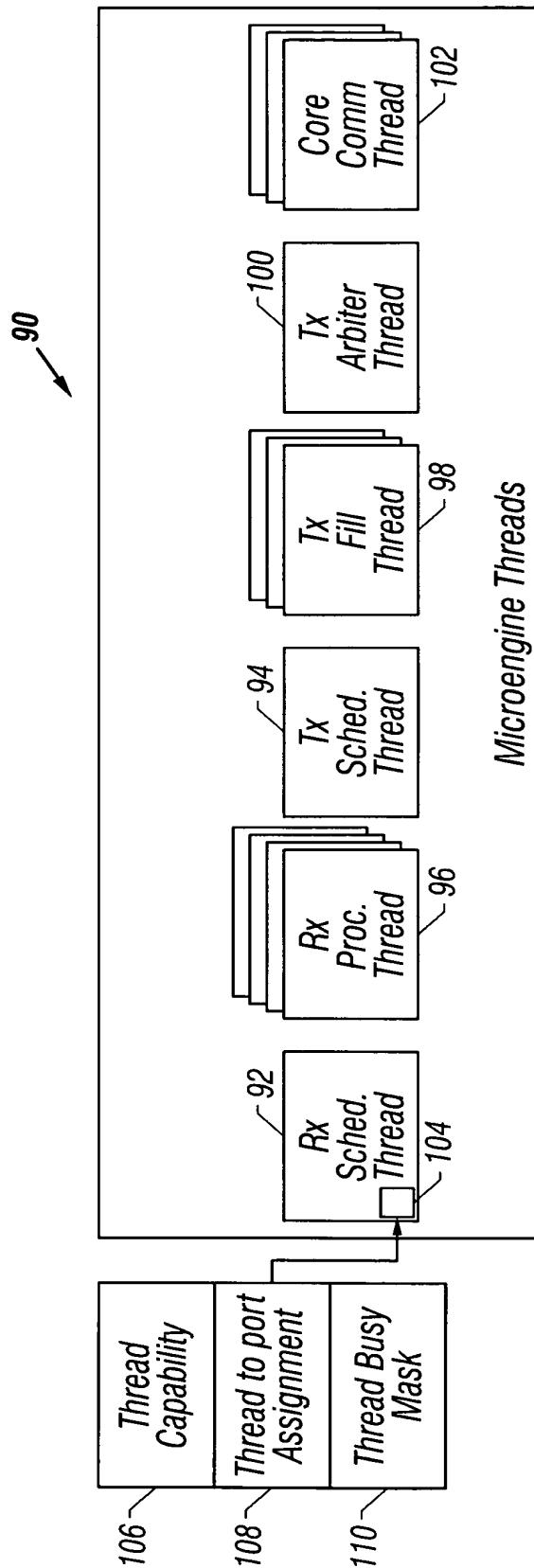


FIG. 3

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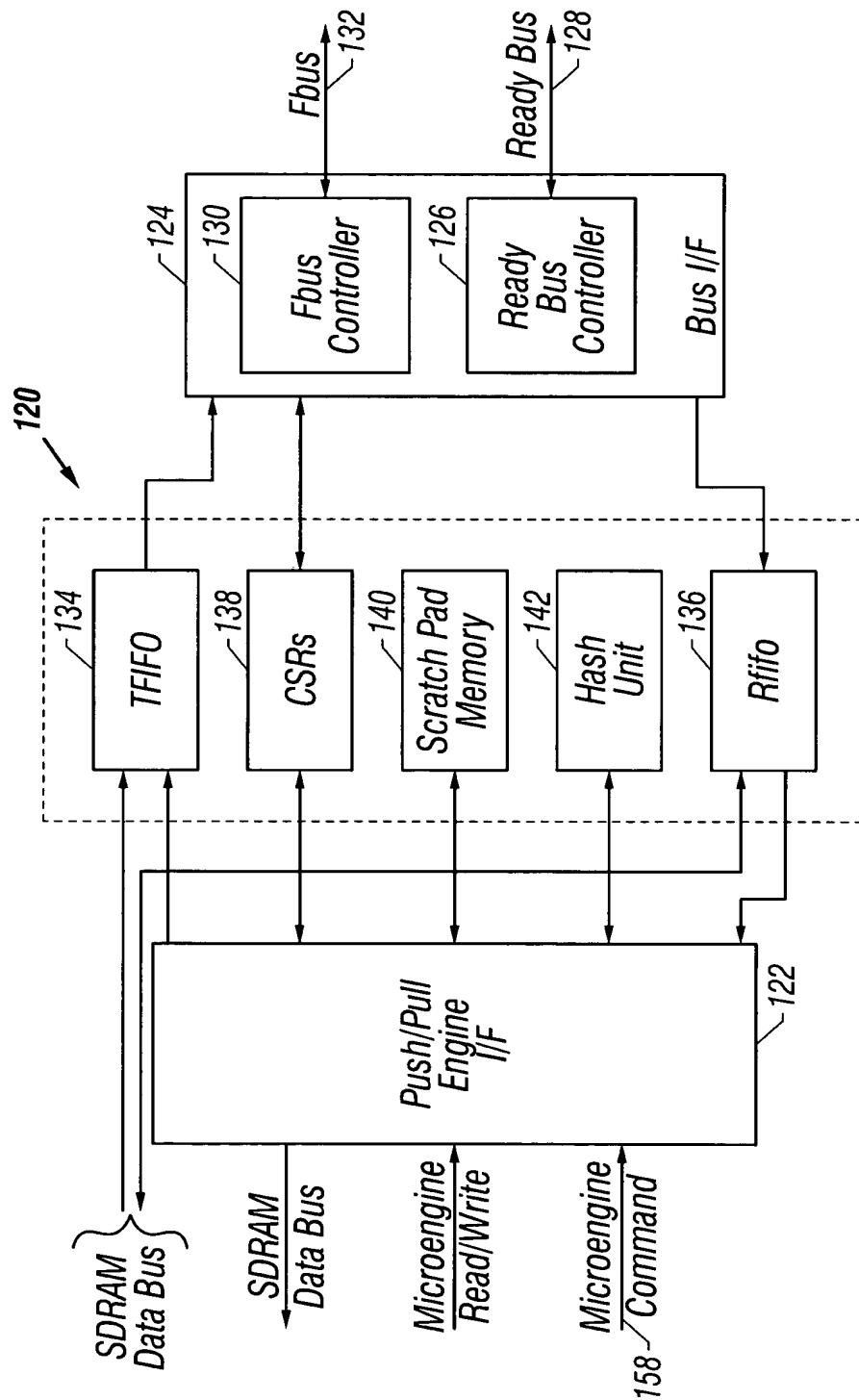
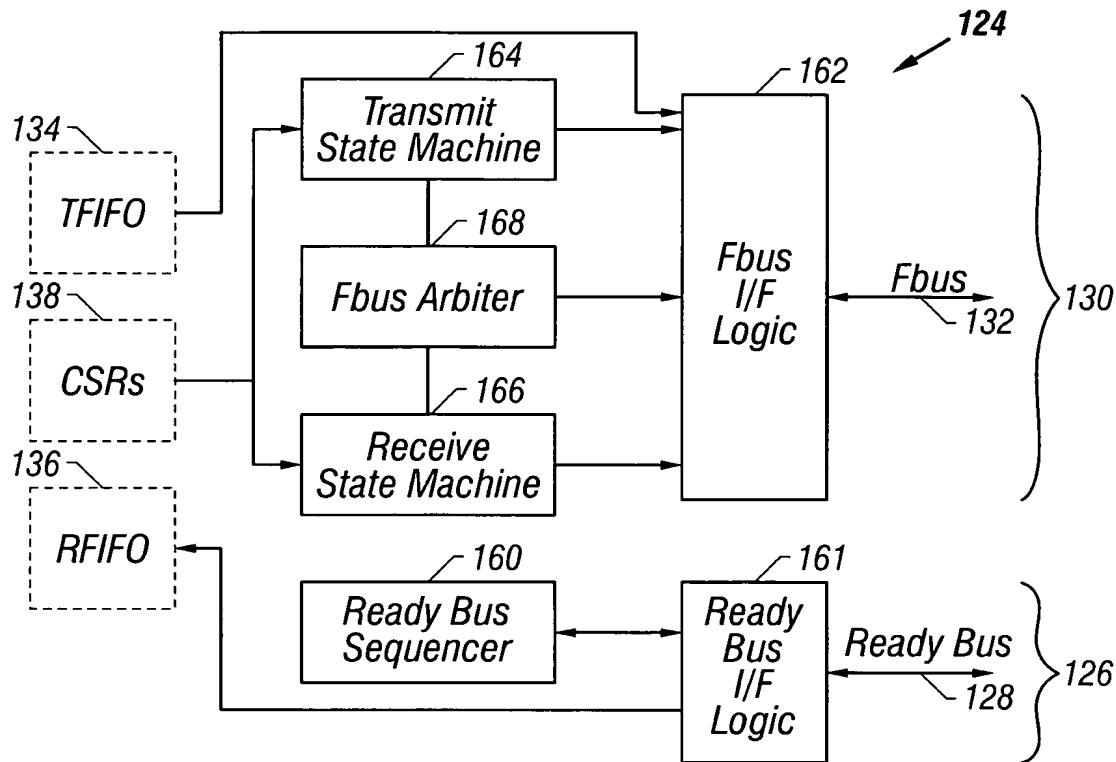
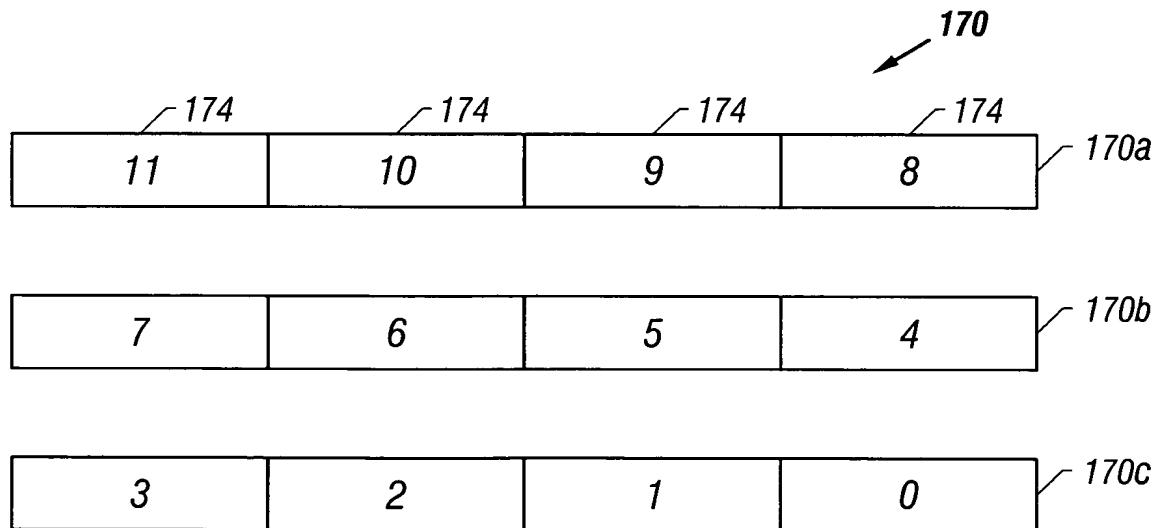


FIG. 4

6/20**FIG. 5****FIG. 6A**

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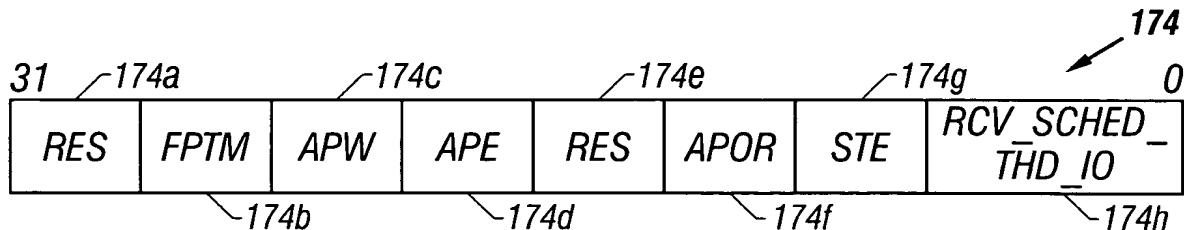


FIG. 6B

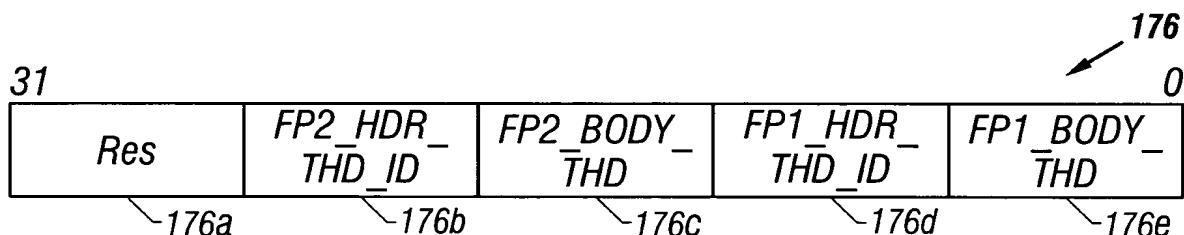


FIG. 6C

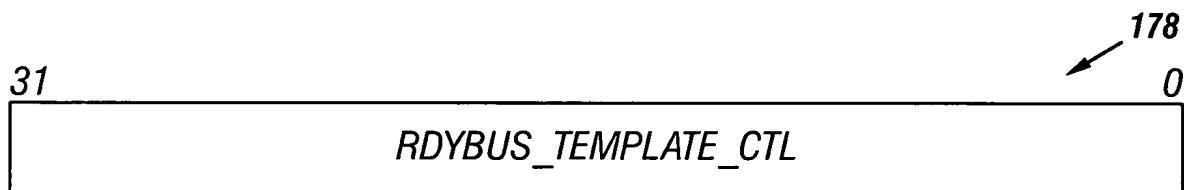


FIG. 6D



FIG. 6E



FIG. 6F

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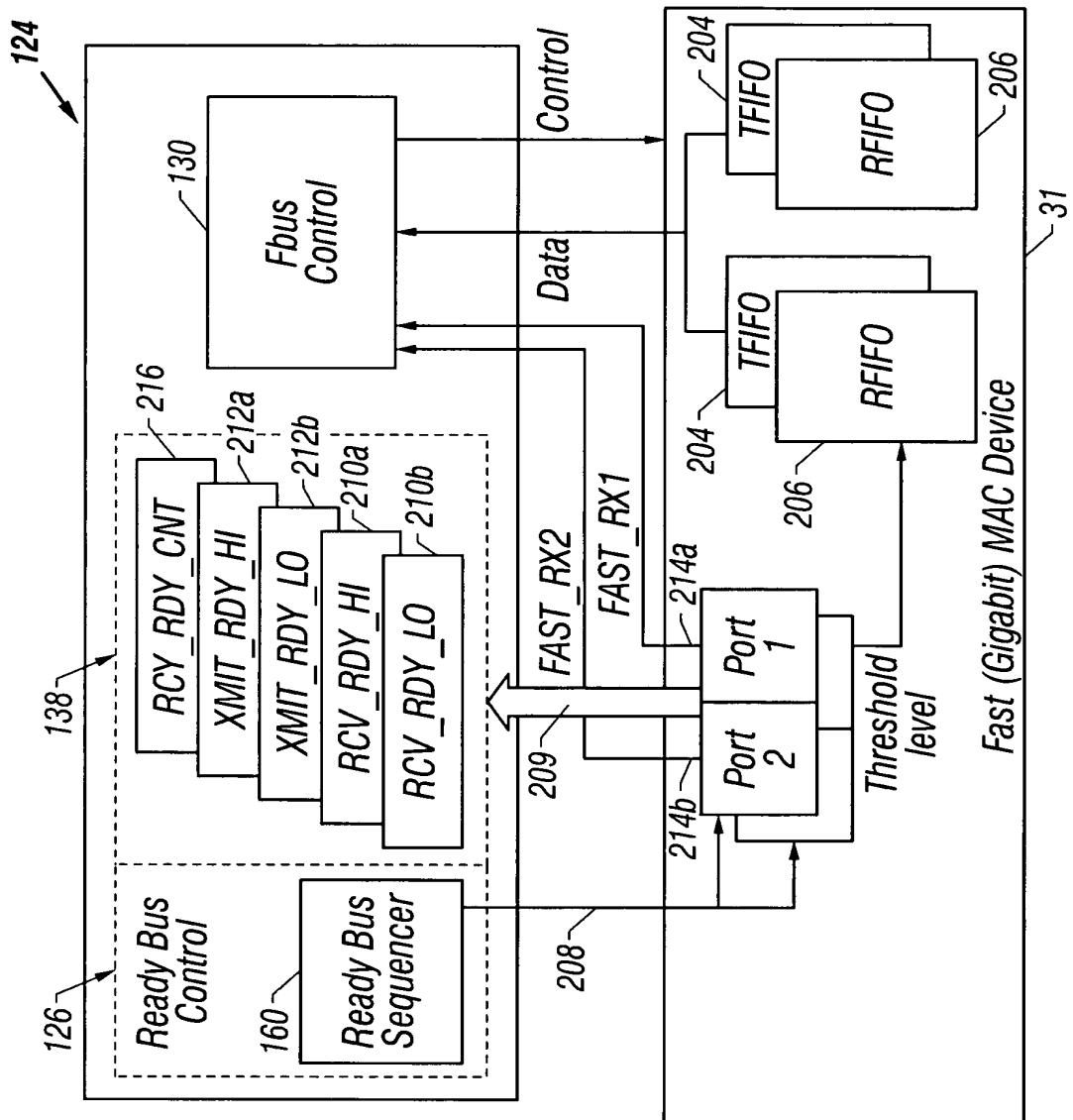
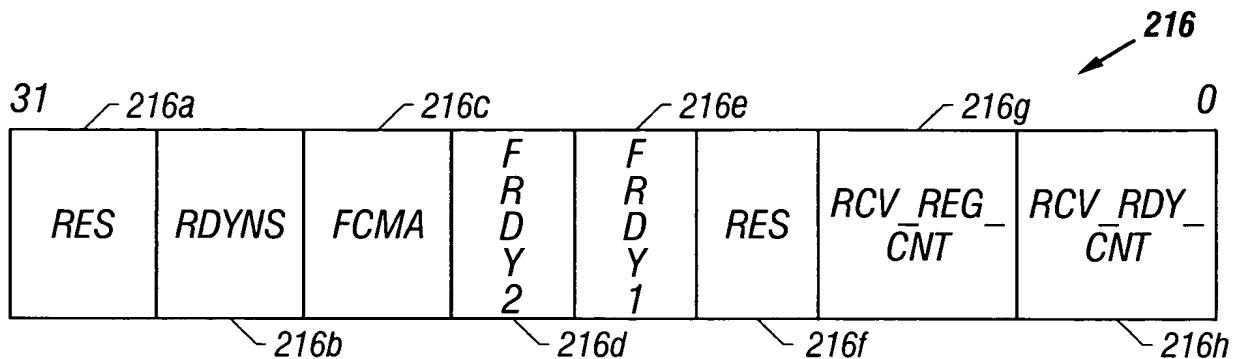
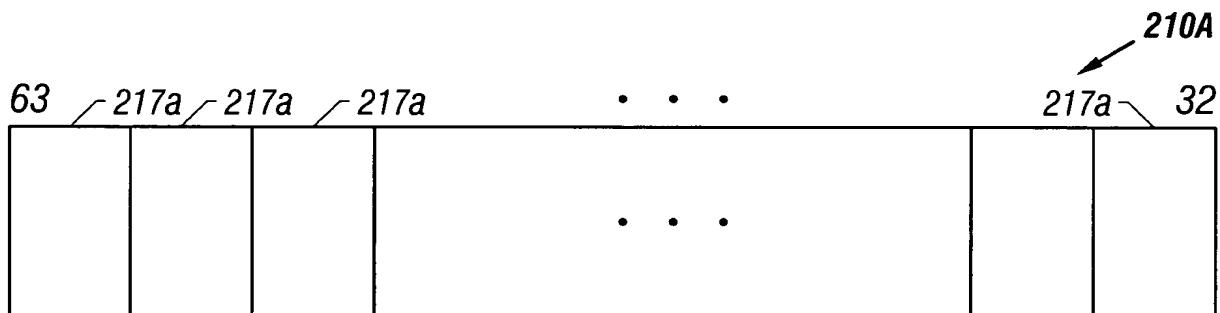
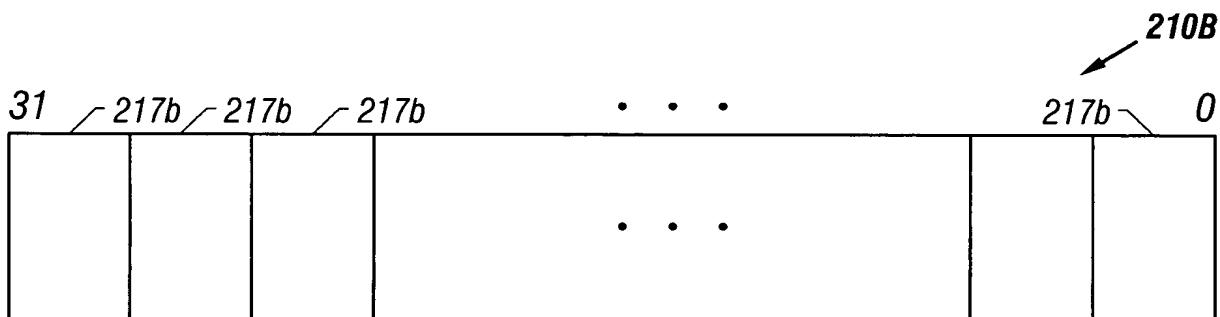


FIG. 7

9/20**FIG. 8A****FIG. 8B****FIG. 8C**

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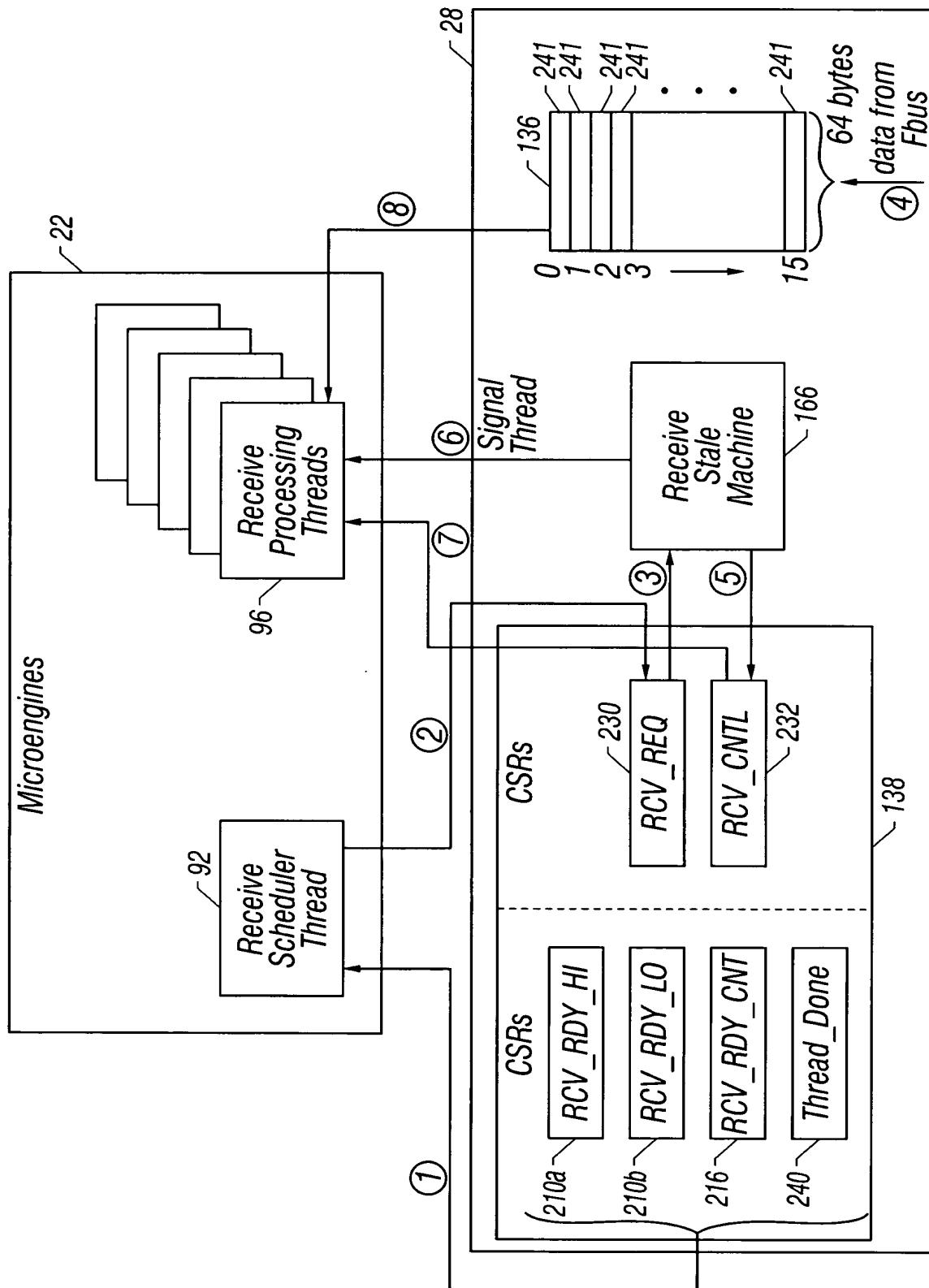


FIG. 9

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230 ↙

RES	FA	THSG	SL	E2	E1	FS	NFE	IGFR	SIGRS	TID	RM	RN	0
													1

231 ↗

FIG. 10A

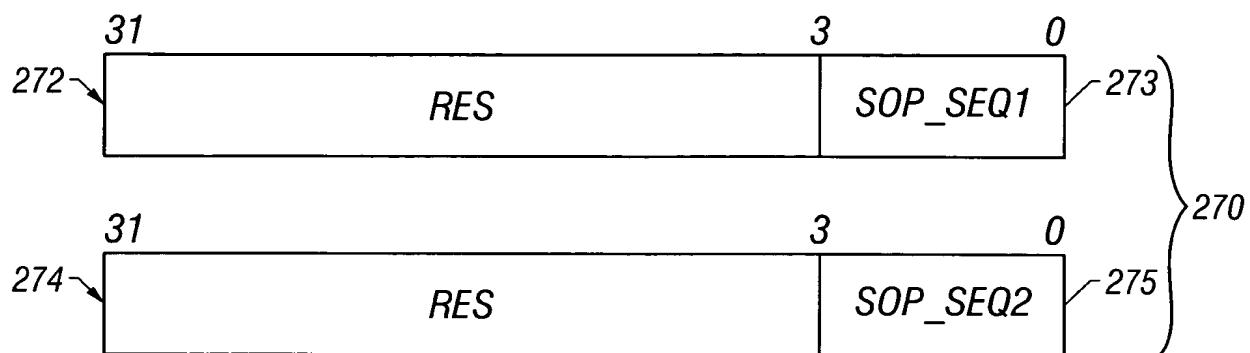
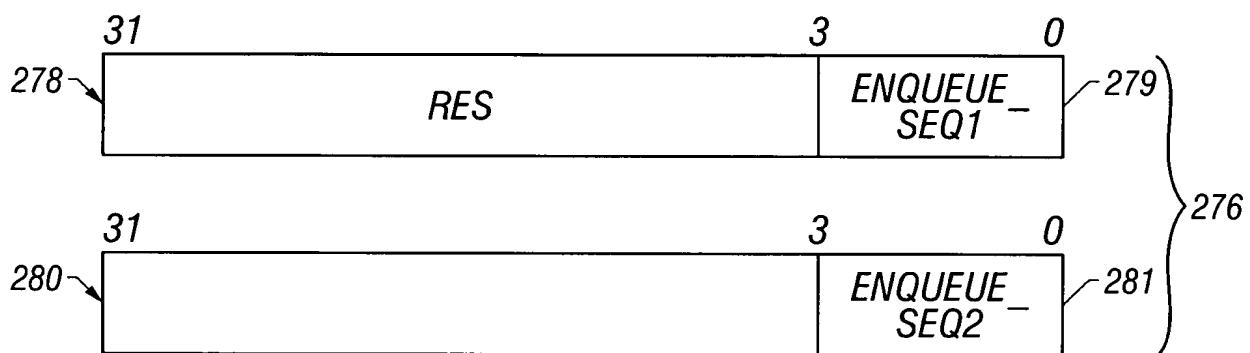
232 ↙

THMSG	MAC-PORT/ THD	SOP SEQ#	RF	RERR	SE	FF	EF	SN	Valid Bytes	EOP	SOP	0
												1
												2
												3

233 ↗

233 ↗

FIG. 10B

12/20**FIG. 11A****FIG. 11B**

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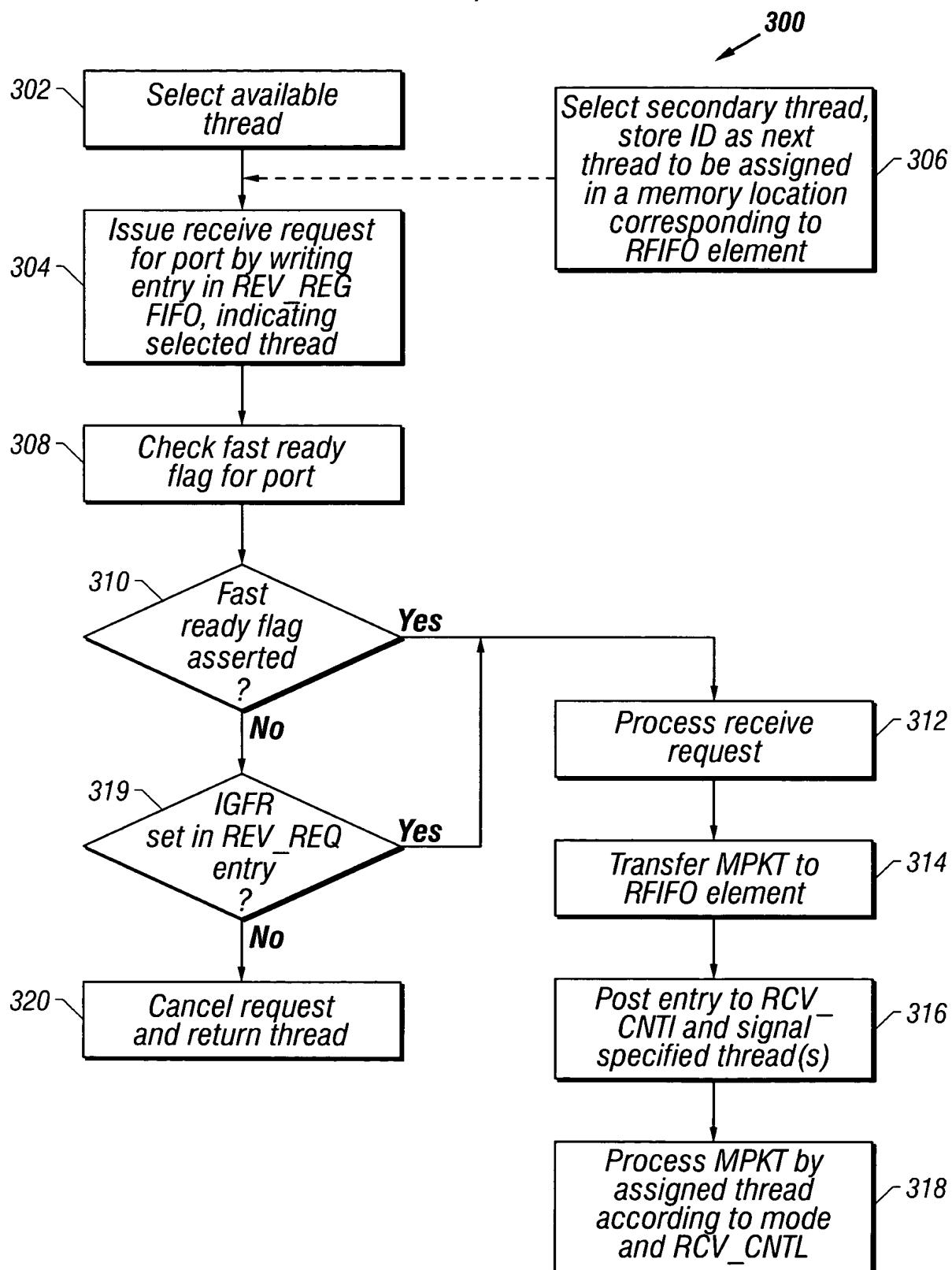


FIG. 12

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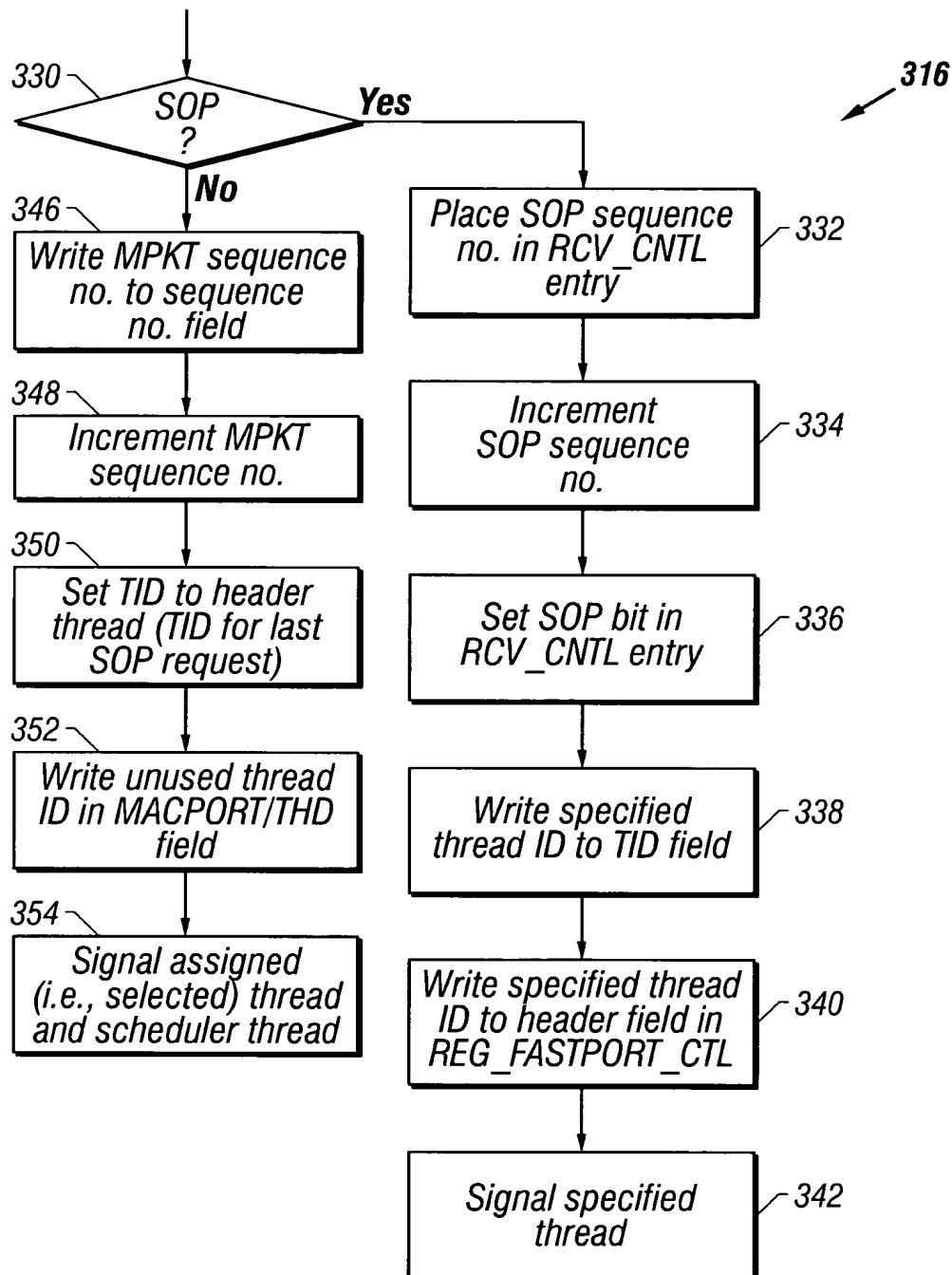
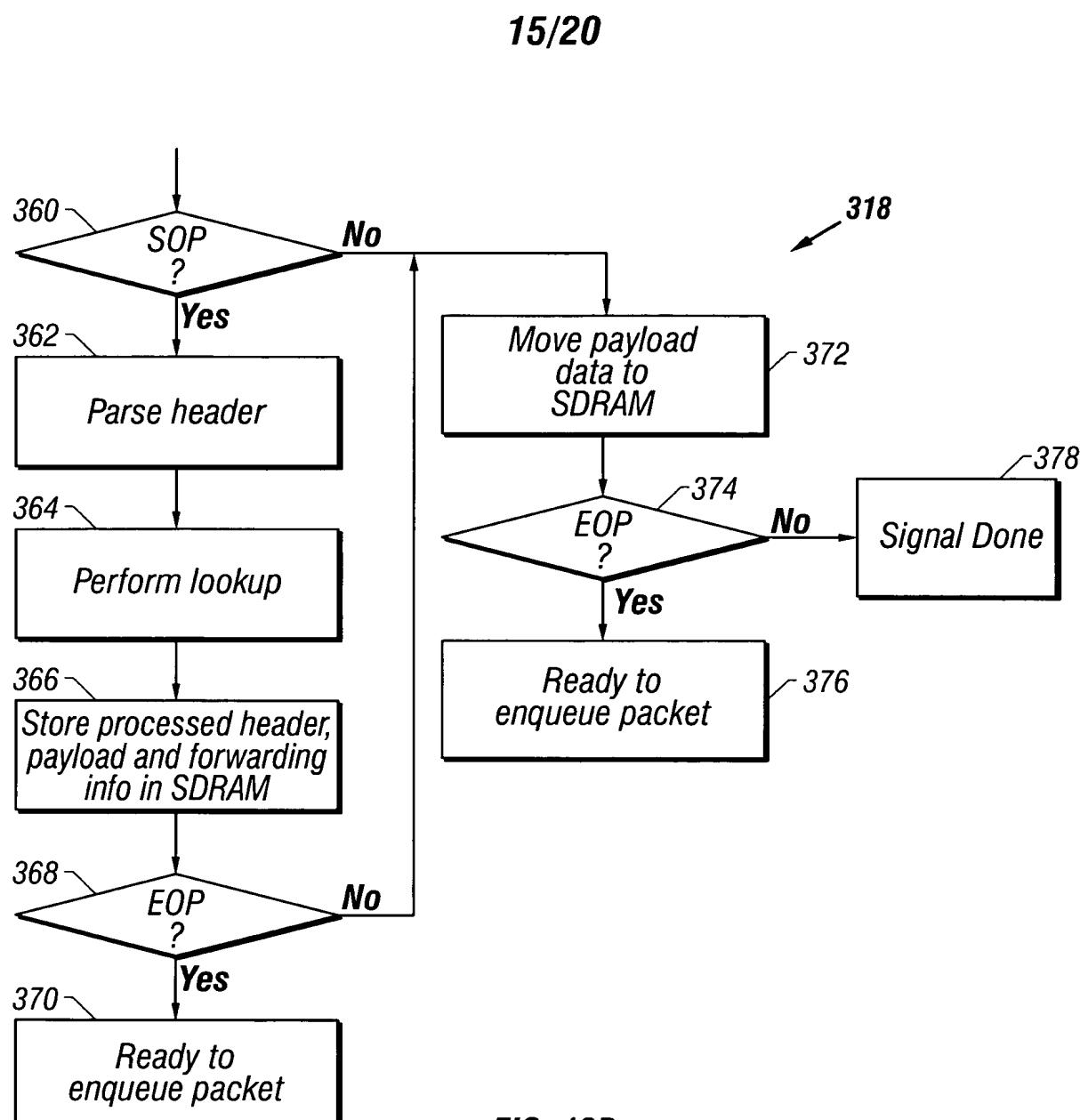


FIG. 13A

**FIG. 13B**

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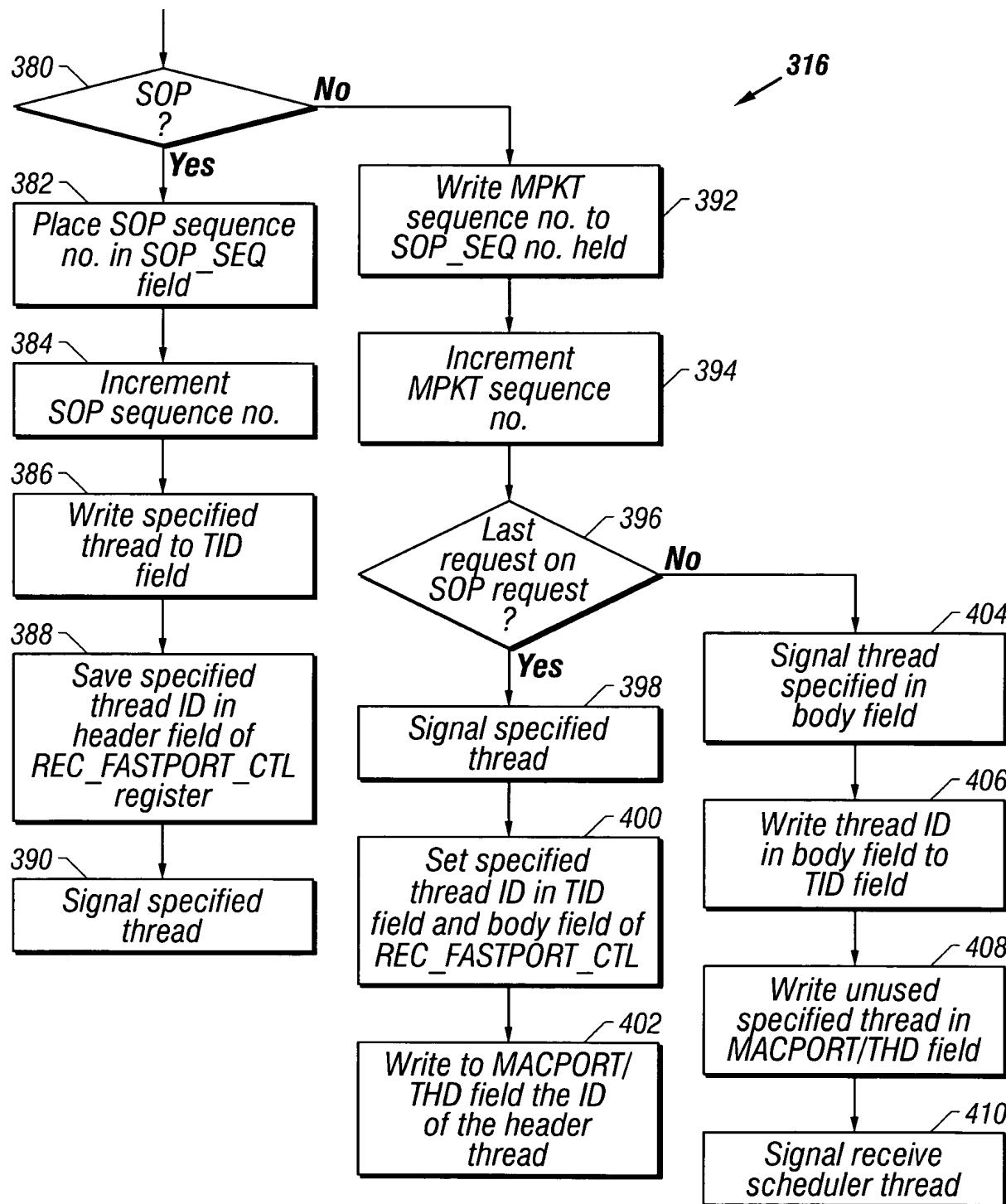
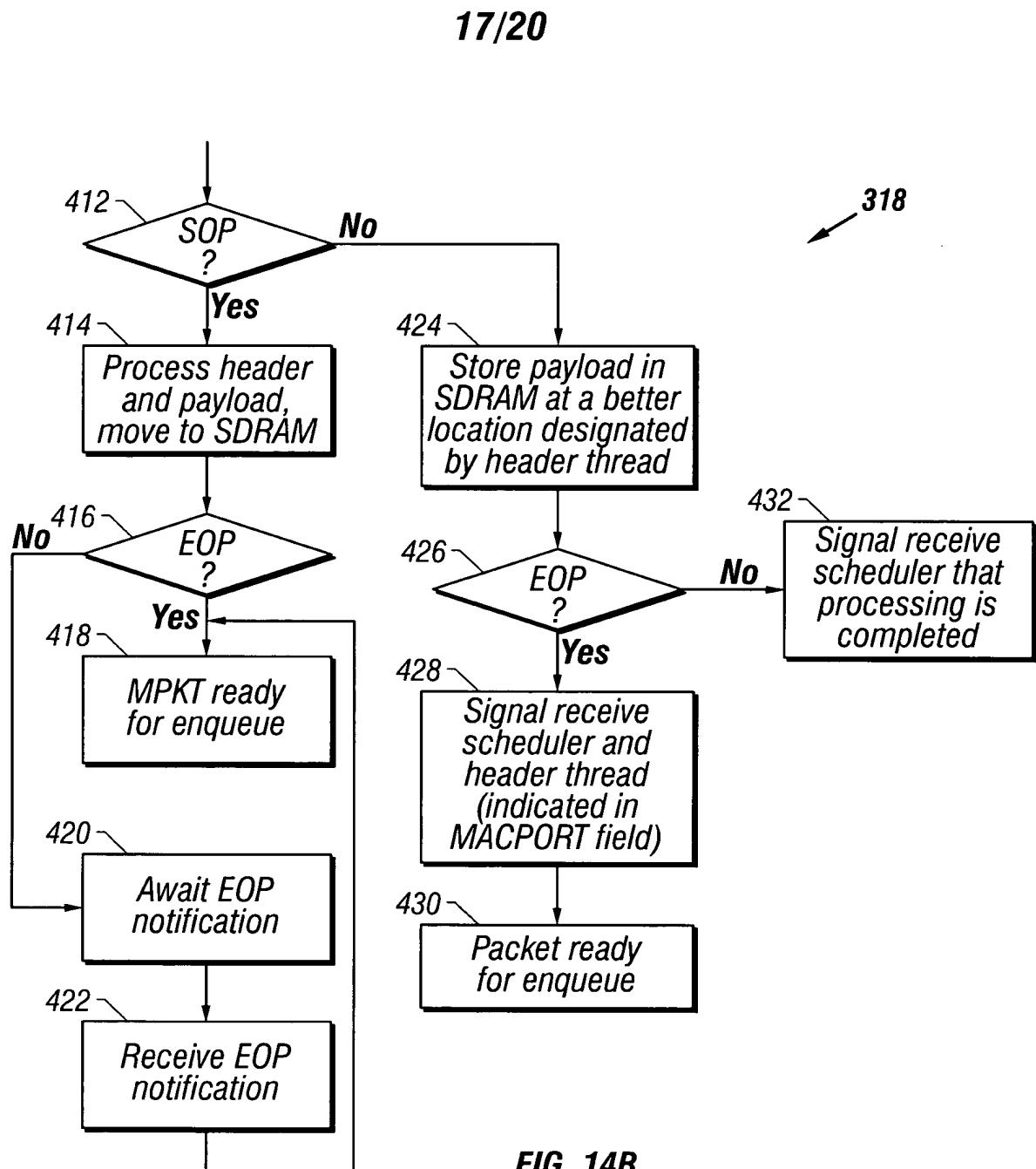
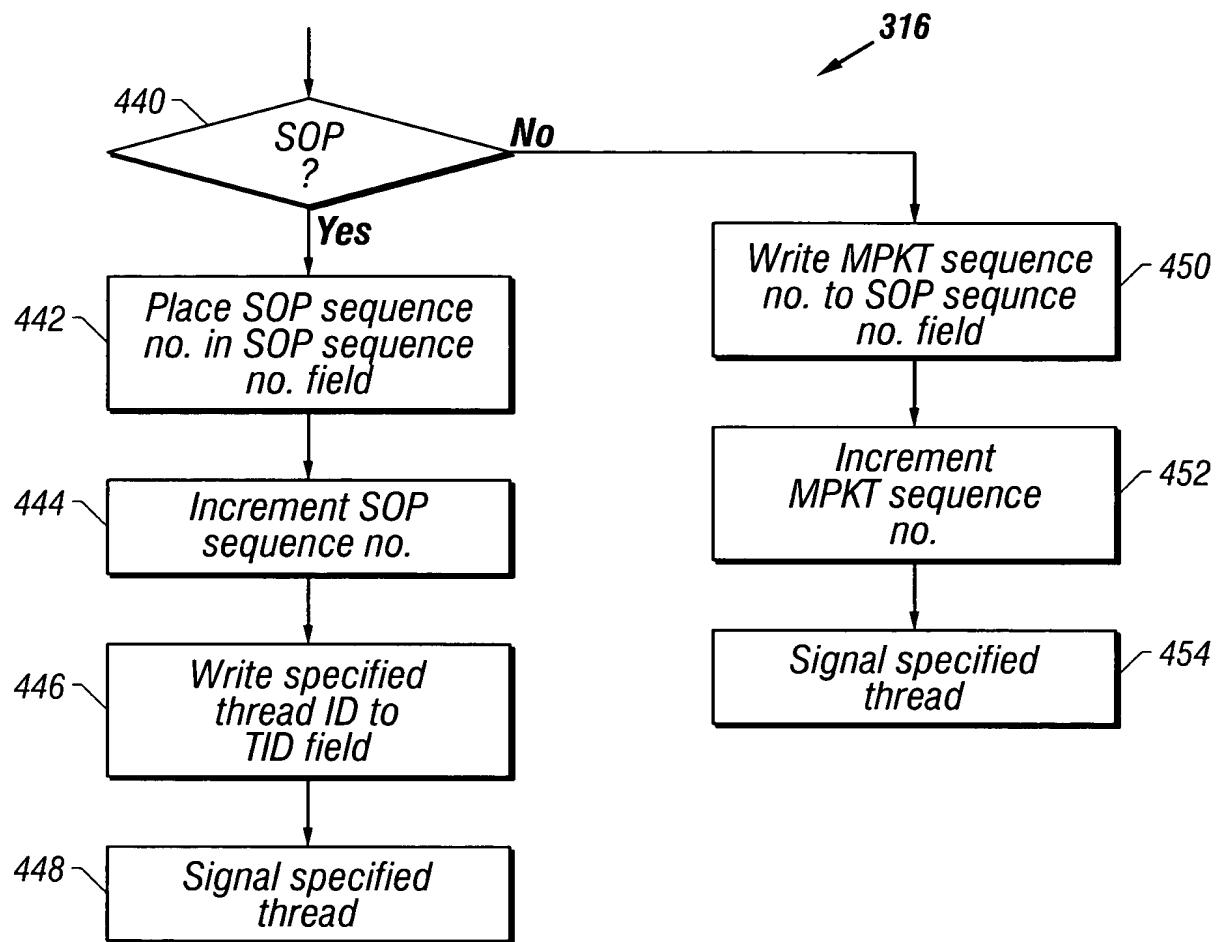


FIG. 14A

**FIG. 14B**

18/20**FIG. 15A**

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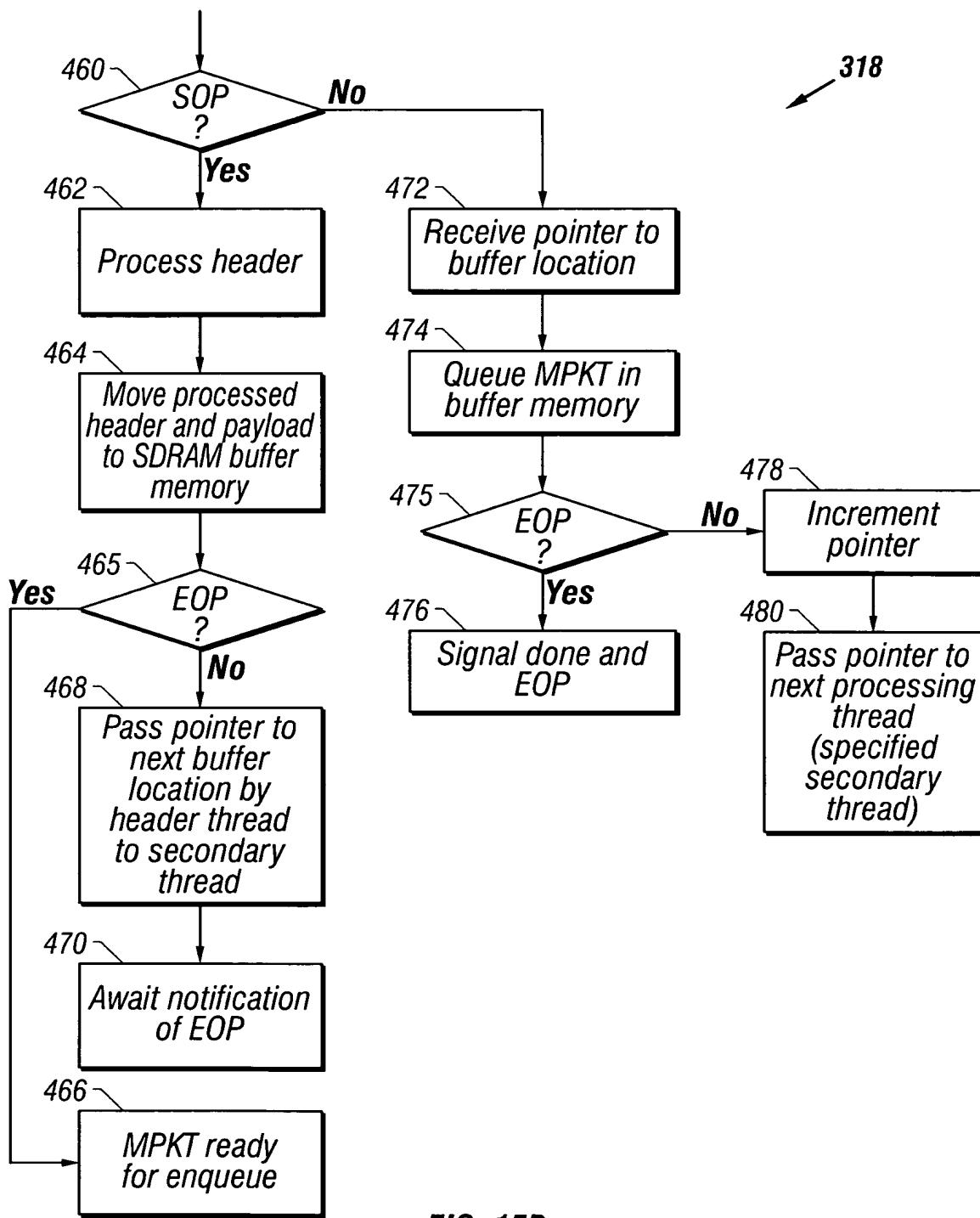
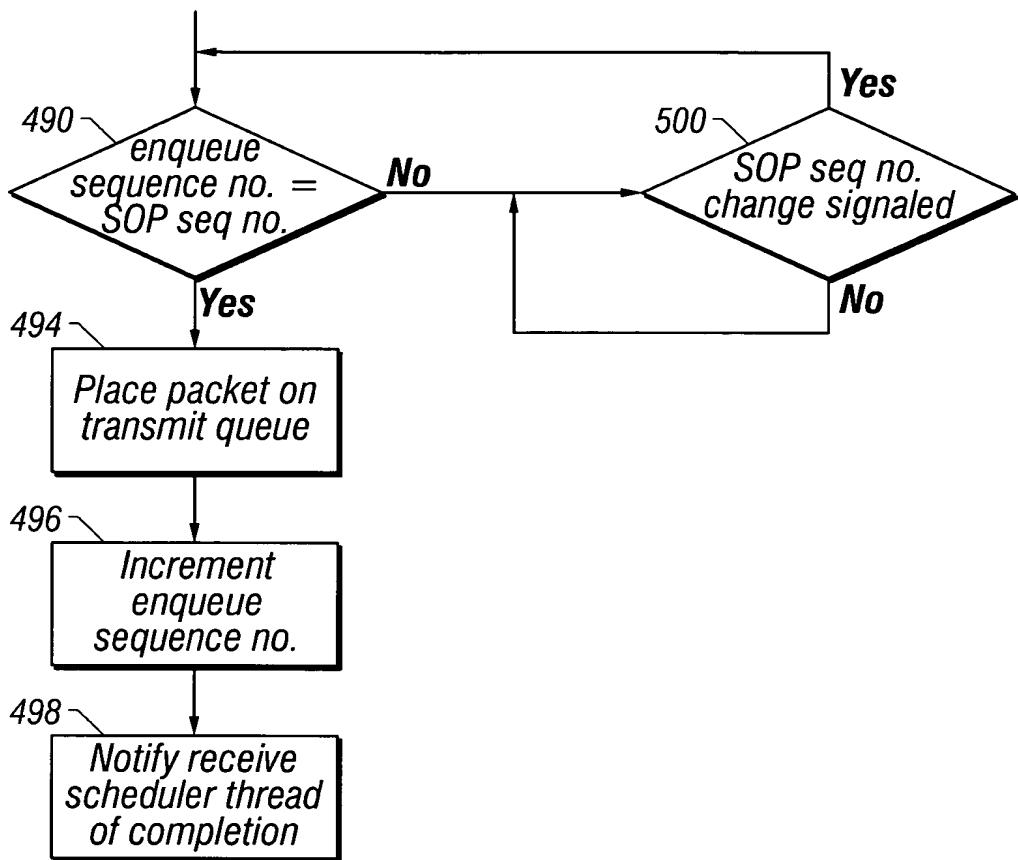


FIG. 15B

20/20**FIG. 16**